FDP-166	VERILOG PROGRAMMING AND IMPLEMENTATION IN FPGA	31.12.2018 to 04.01.2019

OBJECTIVES:

- Write Verilog programs to develop combinational and sequential digital circuits
- Simulate the Verilog program
- Synthesis the circuits in FPGA
- Implement real-time applications in FPGA

PARTICIPANTS:

Teachers of Electrical, Electronics & Communication and Instrumentation disciplines having digital electronics knowledge.

INPUT:

Digital design with Verilog language – Hierarchical modeling – basic Concepts – Modules and Ports – Gate Level Modeling – Data Flow Modeling – Behavioural level Modeling – Combinational circuit design – Sequential circuit design - Finite State Machine - Memory – Applications - Simulation – Test Bench Code - Synthesis in FPGA.

PROCESS:

- Lecture
- Demonstration
- Laboratory sessions

OUTPUT:

The Participants will be able to write Verilog program for digital logic circuits and implement using FPGA.

RESOURCE PERSONS:

- Dr. G.A. Rathy
- Guest Faculty

COORDINATOR	VENUE	LAST DATE FOR RECEIPT OF APPLICATIONS
Dr. P. Sivasankar	NITTTR , Chennai	15 days prior to the start of the programme