

FDP-12	VERILOG PROGRAMMING AND IMPLEMENTATION IN FPGA	20.05.2019 to 24.05.2019
<p>OBJECTIVES:</p> <ul style="list-style-type: none"> ➤ Write Verilog programs to develop combinational and sequential digital circuits ➤ Simulate the Verilog program ➤ Synthesis the circuits in FPGA ➤ Implement real-time applications in FPGA <p>PARTICIPANTS:</p> <p>Teachers of Electrical, Electronics & Communication and Instrumentation disciplines having digital electronics knowledge.</p> <p>INPUT:</p> <p>Digital design with Verilog language – Hierarchical modeling – basic Concepts – Modules and Ports – Gate Level Modeling – Data Flow Modeling – Behavioural level Modeling – Combinational circuit design – Sequential circuit design - Finite State Machine - Memory – Applications - Simulation – Test Bench Code - Synthesis in FPGA.</p> <p>PROCESS:</p> <ul style="list-style-type: none"> ➤ Lecture ➤ Demonstration ➤ Laboratory sessions <p>OUTPUT:</p> <p>The Participants will be able to write Verilog program for digital logic circuits and implement using FPGA.</p> <p>RESOURCE PERSONS:</p> <ul style="list-style-type: none"> ➤ Dr. G A. Rathy ➤ Guest Faculty 		
COORDINATOR	VENUE	LAST DATE FOR RECEIPT OF APPLICATIONS
Dr. P. Sivasankar	NITTTTR , Chennai	30 days prior to the start of the programme